

Product Brief: AMD EPYC™ Embedded 3000 Family

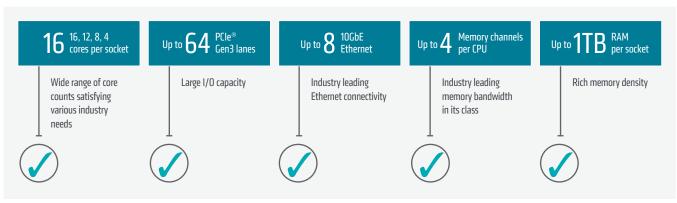
# Breakthrough Performance, Dependability and Security for the Next Generation of Networking, Storage and Industrial Computing Infrastructure

#### **Product Overview**

AMD EPYC™ Embedded 3000 processors expand the AMD EPYC™ Embedded family of products to harness the breakthrough performance benefits of the "Zen" CPU architecture, bringing exceptional reliability, availability and serviceability features to networking, storage and industrial applications. Leveraging major advancements in I/O integration, flexibility, and security capabilities, AMD EPYC™ Embedded 3000 processors set a new benchmark for innovation and performance-per-watt, giving system designers a compelling and cost-effective new choice in x86 embedded processing.

With expansive integrated I/O, true Simultaneous Multithreading (SMT), comprehensive built-in security, and a scalability pathway from AMD EPYC™ Embedded 3000 to data center-class AMD EPYC™ Embedded 7000 processors, system designers can meet and even surpass their ambitious design goals for next-generation network function virtualization (NFV), software defined networking (SDN), networked storage infrastructure, and a wide range of industrial applications.

#### **Outstanding Performance for Wide Applications**



EPYC™ Embedded with 4 memory channels at 2666, theoretical memory bandwidth is up to 85.3GB/s, Xeon-D Broadwell with 2 memory channel at 2400, theoretical memory bandwidth is up to 38.4GB



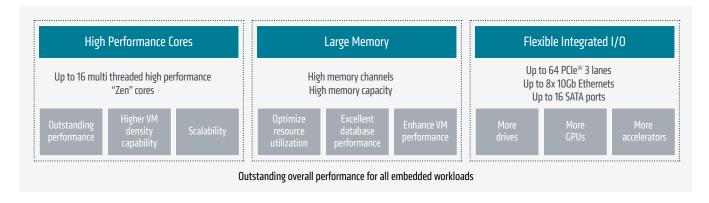


#### A New Benchmark for Performance

AMD EPYC™ Embedded 3000 processors leverage AMD's advanced "Zen" architecture and 14nm FinFET process to deliver up to a 52% improvement in instructions per clock (IPC) compared to legacy architectures¹. System designers can

exploit high-speed single-thread processing performance and/ or multithread processing leveraging up to 16 cores to accelerate throughput for their unique application requirements.

#### **Enhance Performance**

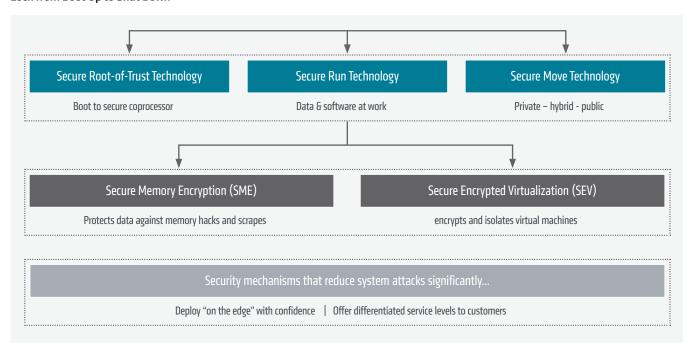


# **Advanced Security Features**

AMD EPYC™ Embedded 3000 processors feature an onboard AMD Secure Processor for Crypto Co-processing that encrypts data before it feeds to the I/O, complemented with Hardware Validated Boot capabilities to ensure systems are booted from trusted software, with one-time programmable (OTP) capabilities enabling system designers' unique configuration.

Advanced capabilities include Secure Memory Encryption (SME) for defending against unauthorized memory access, and Secure Encrypted Virtualization (SEV) for securely isolating hypervisors and virtual machines (VMs) – with no application code changes required.

#### Lock from Boot Up to Shut Down





## **Enterprise-Class Data Integrity**

AMD EPYC™ Embedded 3000 processors provides world class, enterprise-class reliability, availability and serviceability features to provide error detection, correction, recovery and containment, helping ensure high data integrity for the most stringent applications. The availability features in AMD EPYC™ Embedded processors are designed to ensure that applications stay online

and accessible to users even in the presence of uncorrectable errors. Enhanced serviceability features address the need to enable servicing to happen at preplanned times, accelerating troubleshooting and helping reduce downtime.

### **RAS Features Summary**

#### Reliability

- Low-SER FinFET Transistors
- · Parity and error-tolerant devices throughout core
- Caches
  - L1 data cache with SEC-DED ECC
  - L1 data tag / L1 instruction cache with parity + retry
  - L2 / L3 caches with DEC-TED ECC
- DRAM
  - DRAM ECC with Chipkill capabilities
  - DRAM Address/Command Paroty with Replay
  - DRAM Write Data CRC with Replay
- CRC protection of core data buses
- · Parity on all internal data buses
- Link Packet CRC with Retry
- Sync Flood on uncontainable errors
- PCIe® Advanced Error Recovery (AER)
- PCIe® Downstream Port Containment (DPC)

#### **Availability**

- Machine Check Recovery on uncorrectable errors
- Error Thresholding for Predictive Failure Analysis
- · NVDIMM support
- Watchdog timers
- · Core disable
- PCIe® Non-Transparent Bridging (NTB)

#### Serviceability

- Machine Check Architecture Extensions (MCAX)
  - · Scalable MCA
  - First Error Diagnosability
  - DOER/SEER architecture
- DDR4 Post Package Repair (boot time)
- · Platform First Error Handling
- APML SB-RMI, notification on errors
- L2, L3, and DRAM scrubbers
- · DRAM Error Injection

# **Additional Key Benefits**

- Single-thread and multithread processing agility spans from 4 to 16 core configurations, with TDPs ranging from 30W to 50W (1 die, up to 8 cores), and 65W to 100W (2 dies, up to 16 cores).
- Provides up to 64 PCle® lanes in 2 die configurations, with up to 8 channels of 10 GbE, and up to 32MB shared L3 cache with up to 4 independent memory channels.
- Integrated eight 10Gb ethernet ports provide seamless support for IPv4 and IPv6 security protocols, with integrated crypto acceleration supporting the IPsec protocol.
- Up to 64 lanes of PCIe® connectivity in the 2 die configurations, which can be configured as 16 lanes of SATA connectivity enable expanded support for NVMe and SATA-connected storage devices.
- Ideally suited for rugged applications in industrial segments via a robust BGA package with pin-compatibility options from 4 to 16 cores to enable multiple rugged designs with one design footprint.
- Planned product availability extends up to 10 years, providing customers with a long-lifecycle support roadmap.



# **Target Applications**



#### Networking

- Highly parallelized CPU ideal for Network Function Virtualization (NFV) and Software Defined Network (SDN)
- Security for business critical network data
- · HW encrypted multi-tenant security
- High I/O for network connectivity
- Memory capacity for large traffic datasets



#### Industrial

- High integer and floating point capacity
- Enterprise level RAS (Reliability, Accessibility and Serviceability) to maximize uptime
- Flexible stack to minimize the solution development and deployment
- · Security for business critical data



#### Storage

- Direct SATA & NVMe Support
- High parallelism for low latency More memory for larger cache
- High I/O bandwidth for faster data loading
- Memory encryption for data security

Model #	Cores	Threads	TDP (W)	Base Freq (Ghz)	All Cores Boost Freq (Ghz)	Max. Boost Freq (Ghz)	L3 \$ (MB)	DDR Channels	Max DDR Freq (1DPC)	PCle®	Tj (C)
3451	16	32	100	2.15	2.45	3.00	32	4	2666	x64	95
3401	16	16	85	1.85	2.25	3.00	32	4	2666	x64	105
3351	12	24	80	1.90	2.75	3.00	32	4	2666	x64	95
3301	12	12	65	2.00	2.15	3.00	32	4	2666	x64	95
3251	8	16	55	2.50	3.10		16	2	2666	x32	105
3201	8	8	30	1.50	3.10		16	2	2133	x32	95
3151	4	8	45	2.70	2.90		16	2	2666	x32	95
3101	4	4	35	2.10	2.90		8	2	2666	x32	95

For more information about the specific features and specifications supported by select products in AMD's solutions portfolio, or to learn more about AMD's EPYC™ Embedded 3000 Family, visit **www.amd.com/epycembedded** 

# AMD.com/embedded

1. Generational IPC uplift for the "Zen" architecture vs. "Piledriver" architecture is +52% with an estimated SPECint\_base2006 score compiled with GCC 4.6 -02 at a fixed 3.4GHz. Generational IPC uplift for the "Zen" architecture vs. "Excavator" architecture is +64% as measured with Cinebench RT5 TI, and also +64% with an estimated SPECint\_base2006 score compiled with GCC 4.6 -02, at a fixed 3.4GHz. System configs: AMD reference motherboard(s), AMD Radeon" R9 290X GPU, 8GB DDR4-2667 ("Zen")/8GB DDR3-2133 ("Excavator")/8GB DDR3-1866 ("Piledriver"), Ubuntu Linux 16.x (SPECint\_base2006 estimate) and Windows\* 10 x64 RS1 (Cinebench RT5). SPECint\_base2006 estimates: "Zen" vs. "Piledriver" (31.5 vs. 20.7 | +52%), "Zen" vs. "Excavator" (31.5 vs. 19.2 | +64%). Cinebench RT5 1t scores: "Zen" vs. "Piledriver" (139 vs. 79 both at 3.4G | +76%), "Zen" vs. "Excavator" (160 vs. 97.5 both at 4.0C| +64%). G0-108

